

## ABSTRACT OF THE DISCLOSURE

A stacked-gate flash memory cell is provided having step-shaped poly-gates with increased overlap area between them in order to increase the coupling ratio and hence the program speed of the cell. The floating gate is first formed with a step and the intergate dielectric is conformally shaped thereon followed by the forming of the control gate thereon. The increase in the overlap area can be achieved by forming gates with multiply connected surfaces of different shapes.